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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/939,761

08/28/2001

Koji Furusawa

NEC2480-US

3216

466

7590

07/15/2002

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EXAMINER

ORTIZ, EDGARDO

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 07/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.
09/939,761

Applicant(s)
Furusawa

Examiner
Edgardo Ortiz

Art Unit
2815



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Apr 23, 2002
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7-21 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 7-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on Apr 23, 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ 6) ☐ Other:

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DETAILED ACTION

This Office Action is in response to an amendment filed April 23, 2002 on which Applicant canceled claims 1-6 and added new claims 7-21.

Claim Objections

1. Claim 14 is objected to because of the following informalities: In line 12 the claim reads "boding wire" when it should read "bonding wire". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 and 14 recite the limitation "said second semiconductor substrate" in line 11 of claim 8 and line 11 of claim 14. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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Claims 7, 8, 12, 14, 15 and 17 are rejected under 35 U.S.C. 102 (b) as being anticipated by Takiar et.al. (U.S. Patent No. 5,502,289). With regard to claims 7, 12, 15 and 17; Takiar teaches a substrate (142), a first semiconductor chip (136) on said substrate, a second semiconductor chip (140) overlying said first semiconductor chip, a wiring layer (138) between said first and second semiconductor chips, said wiring layer comprising a substrate material which is defined as including a conductor such as copper or aluminum and a dielectric such as a polyimide, a plurality of bonding pads on the wiring layer, the substrate and the first and second semiconductor chips and a plurality of bonding wires for connecting said plural bonding pads to each other. See Figure 7.

With regard to Claims 8 and 14, as best the examiner is able to ascertain the claimed invention, Takiar teaches a first bonding wire that connects one of said plural bonding pads on the substrate (142) to one of the plural bonding pads on the first semiconductor chip (136), a second bonding wire that connects one of the plural bonding pads on the substrate to one of the plural bonding pads on the wiring layer (138) and a third bonding wire that connects one of the plural bonding pads on the wiring layer to one of the plural bonding pads on the substrate.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103 (a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

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such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9, 13 and 19 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takiar et.al. (U.S. Patent No. 5,502,289) in view of Beilstein, Jr. et.al. (U.S. Patent No. 5,567,654).

Takiar, as stated supra, essentially discloses the claimed invention but fail to show, a connection wire for connecting one of the plural bonding pads on the wiring layer to another one of the plural bonding pads on the wiring layer. With regard to Claims 9, 13 and 19; Beilstein teaches an electronic module package that includes an interposer layer (95), comprising a ceramic, having wiring (97) within the interposer and connected to pads (89). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Takiar to include a connection wire for connecting one of the plural bonding pads on the wiring layer to another one of the plural bonding pads on the wiring layer, as clearly suggested by Bielstein, in order to connect the electronic package to external circuitry or lead frame connections.

Claims 10, 11, 16, 18 and 20 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takiar et.al. (U.S. Patent No. 5,502,289) in view of Tokuda et.al. (U.S. Patent No. 5,870,289).

Takiar, as stated supra, essentially discloses the claimed invention but fail to show, a via hole on the wiring layer and connected to a bonding pad of a semiconductor chip. With regard to Claims 10, 11, 16, 18 and 20, Tokuda teaches a chip connection structure having a direct through-hole

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connection (40) through a wiring layer (20) which connects to a bonding pad (11) of an integrated circuit chip (10). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Takiar to include a via hole on the wiring layer and connected to a bonding pad of a semiconductor chip, as clearly suggested by Tokuda, in order to achieve high signal transmission and ensure high reliability by the dispersion of stress.

Claim 21 is rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takiar et.al. (U.S. Patent No. 5,502,289) in view of Tokuda et.al. (U.S. Patent No. 5,870,289) and further in view of Beilstein, Jr. et.al. (U.S. Patent No. 5,567,654). Takiar and Tokuda, as stated supra, essentially disclose the claimed invention but fail to show, a connection wire for connecting one of the plural bonding pads on the wiring layer to another one of the plural bonding pads on the wiring layer. With regard to Claim 21, Beilstein teaches an electronic module package that includes an interposer layer (95), comprising a ceramic, having wiring (97) within the interposer and connected to pads (89). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Takiar and Tokuda to include a connection wire for connecting one of the plural bonding pads on the wiring layer to another one of the plural bonding pads on the wiring layer, as clearly suggested by Bielstein, in order to connect the electronic package to external circuitry or lead frame connections.

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Response to Arguments

4. Applicant's arguments with respect to claims 7-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call

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Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

7/10/02

A handwritten signature in black ink, appearing to be 'E. Lee', written in a cursive style.

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800